DOCKET NO. 99-102/1D

**In the Specification:**

Please replace the first paragraph inserted after the title and subtitle by the Preliminary Amendment filed with the patent application on March 15, 2002, with the following rewritten paragraph:

B1

-- This application is a division of U.S. Patent 6,391,795 B1, issued May 21, 2002. --

Please replace the third of the three paragraphs inserted after the title and subtitle by the Preliminary Amendment filed with the patent application on March 15, 2002, with the following rewritten paragraph:

B2

--The subject matter of this application relates to the subject matter of Li, Catabay, and Hsia U.S. Patent No. 6,423,628, issued July 23, 2002, entitled "INTEGRATED CIRCUIT STRUCTURE HAVING LOW DIELECTRIC CONSTANT MATERIAL AND HAVING SILICON OXYNITRIDE CAPS OVER CLOSELY SPACED APART METAL LINES", filed by one of us with others on October 22, 1999, assigned to the assignee of this application, and the subject matter of which is hereby incorporated herein by reference.--

Please replace the paragraph beginning at page 3, line 27, in the parent application with the following rewritten paragraph:

--In the aforementioned U.S. Patent No. 6,423,628, issued July 23, 2002, a layer of silicon oxynitride (SiON) is formed over the top surface of the metal lines to serve as an anti-reflective coating (ARC), a hard mask for the formation of the metal lines, and a buffer layer for chemical mechanical polishing (CMP). Low k silicon oxide dielectric material having a high carbon doping level is then formed in the high aspect regions between closely spaced apart metal lines up to the level of the silicon oxynitride. CMP is then applied to planarize the upper surface of the low k carbon-doped silicon oxide dielectric layer, using the SiON layer as an etch stop, i.e., to bring the level of the void-free low k silicon oxide dielectric layer even with the top of the SiON layer. A conventional (non-low k) layer of silicon oxide dielectric material is then deposited by plasma enhanced chemical vapor deposition (PECVD) over the low k layer and the SiON layer. A via is then cut through the second dielectric layer and the SiON to the top of the metal line. Since the via never contacts the low k layer between the metal lines, via poisoning due to exposure of the low k layer by the via does not occur.--

## REMARKS

Claims 15-19 are now in the application.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached pages are captioned "**Version with marking to show changes made.**"

## I. SUMMARY OF THE JANUARY 31ST, 2003 OFFICE ACTION

Claims 15-19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng U.S. Patent 5,821,621.